What do the delays for memories mean? How to calculate what's necessary?

--DELAYS FOR DATA ARRAYS (64 is 10 says V)

CONSTANT DELAY\_128B : TIME := 14 NS;

CONSTANT DELAY\_256B : TIME := 20 NS;

CONSTANT DELAY\_512B : TIME := 25 NS;

CONSTANT DELAY\_1KB : TIME := 35 NS;

CONSTANT DELAY\_2KB : TIME := 45 NS;

CONSTANT DELAY\_4KB : TIME := 60 NS;

^These are BYTES. You calculate the total cache/array size by multiplying the number of lines in the array by the size of each line.

During ICache fetching for PC, in parallel query BTB and BHT for PC+2 for the next instruction.

BHT is a bimodal predictor. Sufficient? YES

Perf counters: 32-bit incrementing counter. Use two counters to show, e.g., miss count and total count?

BTB is direct mapped cache of some large size (without?) tags. It stores conditional/unconditional bit along with the 16-bit predicted address and valid bit. Stores/overwrites new values when and only when the MEM stage says that the instruction it's looking at was a branch of some sort.

If the valid bit is set, then

if the unconditional bit is set,

use the BTB value as the next PC address,

else the conditional bit must be set, so

check whether the BHT predicts that the BTB prediction should be taken or not

BTB

INPUT:

Curr\_PC, EX\_PC, EX\_target\_actual, EX\_conditional, EX\_write (any branch type is in EX)

OUTPUT:

Valid, Conditional, PredictedTarget

Need to make sure that branch can override all of these conditions (flush).

BHT is a large direct mapped ... cache/dataarray without tags? It stores a just a 2-bit state machine initialized to weakly taken ("10"). The state machine is updated with the taken direction only on conditional branches. (Unconditional branch info is stored entirely in BTB).

\*We might get 5 pts for including them in the same component

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Notes

NOP should not be treated as a branch. Needs to be detected as such.

Fix STB source generation to include forwarding. Move the generation from EX to MEM, but pass RegB->RegSR in EX still.